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FPGA Implementation of Desensitized Half Band Filters

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----------**Abstract**----------
Half band filters are often used for decimation, interpolation and multirate systems. Hence it is a common component in digital circuitry for communication systems. In this paper we have described the efficient design of the low pass finite impulse response (FIR) half band filter using matlab and implemented on Field Programmable Gate Array (FGPA). And also the filter is built using basic filter building blocks in simulink and simulink simulation results are compared with Xilinx simulation results .The design has been prototyped on an xc6vcx240t-1ff1156 in vertex-6 platform using Integrated Synthesis Environment(ISE) 14.2 tool.

Keywords *: FIR, FPGA, matlab, SDR, simulink.*

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I. INTRODUCTION

Digital filters are often used for two general purposes: separation of signals that have been combined and restoration of signals that have been distorted in the same way. It is well known that a digital filter, when constructed as a cascade of two or more subfilters, can possess the capability of lowering the filter's sensitivity to filter coefficient perturbations. This property has been described in [1], where efficient digital FIR lowpass filters were implemented as a cascade of a multiplierless prefilter and an amplitude equalizer. On similar basis lowpass FIR half band filter is implemented in [2], which can lead to circuits having lower power consumption, higher operating speeds, and smaller IC area.

Our work mainly concentrates on the desensitized half band filters design in matlab and implementation on FPGA. Its implementation on FPGA results in reduced resource requirement as these filters have less number of adders and multipliers as given in [2] and hence these half band filters can be used in digital down converters in software defined radios(SDR) with less hardware requirements. The rest of this work is structured as follows: section II covers the design of desensitized half band filters. Section III covers the simulink implementation of the filter using basic filter building elements such as delay chains, gains and add/sub blocks. Section IV covers the FPGA implementation of the desensitized half band filters. Section V covers the result analysis and finally the concluding remarks.

II. DESENSITIZED HALF BAND FILTERS

An FIR half band filter [3] is an FIR digital filter whose transfer function has the form

$$H(z) = z^{-N}\left(h_0 + \sum_{k=1,3,\ldots}^{N} h_k\,(z^k + z^{-k})\right) \qquad (1)$$

Thus, the half band filter is a symmetric FIR filter of length 2N+1, for odd integer N, with h_k=0 for all even integers K, except for the coefficient at the center h_0 which is non zero. Typically we consider h_0=1/2, and the other h_k coefficients can have any desired values. As described in [2], the desensitized half band filter can be implemented as a prefilter and equalizer cascade provided the transfer function of the overall half band filter have the transfer function of the prefilter as a factor. The transfer function of (1) of an FIR half band filter with center tap h_0=R/2 will possess the factor P(z)= $(1 + z^{-1})(1 + z^{-1})$ if and only if any of the following three conditions hold good:

1) $\left|H(e^{jw})\right| = 0$ at w=π;

2) $\left|H(e^{jw})\right| = R$ at w=0;

3) $h_0 = 2(h_1 + h_3 + ...)$;

Now assuming that our half band filter's transfer function has a factor $(1+z^{-1})$, and let us factor it out of the transfer function $H(z)$. For example as in [2] let us consider the degree-14(15-tap) transfer function and we have

$$\begin{aligned} H(z) = (1+z^{-1})[&h_7 + (-h_7)z^{-1} + (h_7+h_5)z^{-2} + (-h_7-h_5)z^{-3} + (h_7+h_5+h_3)z^{-4} \\ &+ (-h_7-h_5-h_3)z^{-5} + (h_7+h_5+h_3+h_1)z^{-6} + (h_7+h_5+h_3+h_1)z^{-7} \\ &+ (-h_7-h_5-h_3)z^{-8} + (h_7+h_5+h_3)z^{-9} + (-h_7-h_5)z^{-10} + (h_7+h_5)z^{-11} \\ &+ (-h_7)z^{-12} + (h_7)z^{-13}\,] \end{aligned} \quad (2)$$

In the above equation substituting

$$\begin{aligned} a_0 &= h_7 + h_5 + h_3 + h_1 \\ a_1 &= h_7 + h_5 + h_3 \\ a_2 &= h_7 + h_5 \\ a_3 &= h_7 \end{aligned} \quad (3)$$

We get

$$\begin{aligned} H(z) = (1+z^{-1})\{&[a_0 z^{-6} + a_1(z^{-4} - z^{-8}) + a_2(z^{-2} - z^{-10}) + a_3(1 - z^{-12})] \\ &+ z^{-1}[a_0 z^{-6} - a_1(z^{-4} - z^{-8}) - a_2(z^{-2} - z^{-10}) - a_3(1 - z^{-12})]\} \end{aligned} \quad (4)$$

Now further simplifying the equation (4) we get

$$\begin{aligned} H(z) = (1+z^{-1})[&a_0 z^{-6}(1+z^{-1}) + a_1 z^{-4}(1-z^{-4})(1-z^{-1}) + a_2 z^{-2}(1-z^{-8})(1-z^{-1}) + \\ &a_3(1-z^{-12})(1-z^{-1})] \end{aligned} \quad (5)$$

To obtain the frequency response we shall consider filter tap coefficients values employed by analog devices in commercial product [4] $h_0 = 8192$, $h_1 = 4964$, $h_3 = -1102$, $h_5 = 273$, $h_7 = -39$ and it satisfies the condition $h_0 = 2(h_1 + h_3 + ...)$.

The magnitude and phase responses of the 15 tap desensitized half band filter are shown in fig. 1

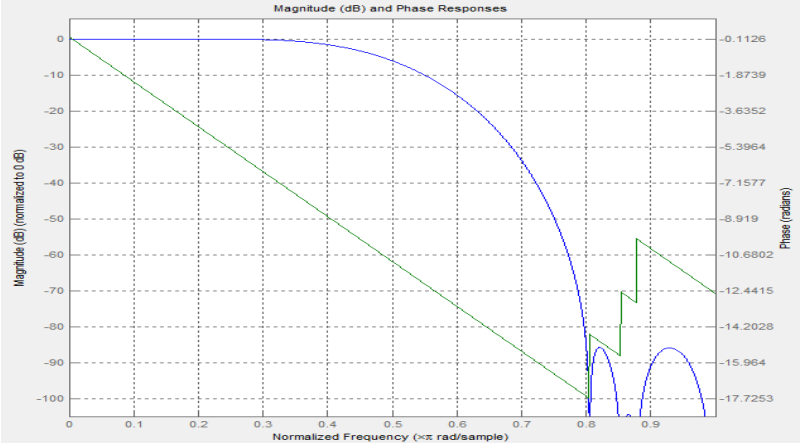

Figure 1:Frequency response of 15 tap desensitized half band filter

The frequency response obtained for 15-tap analog devices [4] and the desensitized half band filter are the same. The pole/zero plot of the desensitized half band filter is shown in fig.2. We have considered tap coefficient values normalized to integer to reduce the complexity of the design. If floating point representation is consider and normalized up to 10 fractional bits we get frequency response as in figure.3 where filter tap coefficient values are $h_0 = 0.5$, $h_1 = 0.3038094552$, $h_3 = -.06815647353$, $h_5 = 0.01611887466$, $h_7 = -0.0036378272$ and the filter's response in stop band deteriorates. The above mentioned design procedure can be applied to half band filters of other lengths in the similar manner.

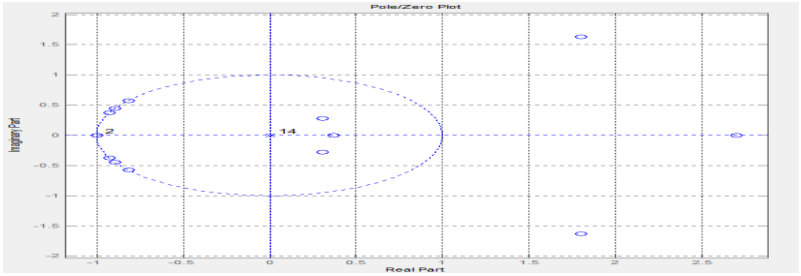

Figure 2:pole/zero plot of 15 tap desensitized half band filter

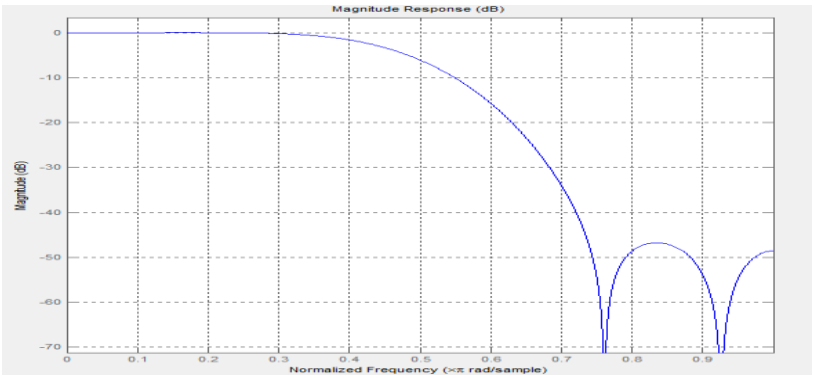

Figure 3:frequency response of 15-tap desensitized half band filter where the filter tap coefficients are taken in floating point representation.

III. IMPLEMENTATION OF DESENSITIZED HALF BAND FILTERS USING SIMULINK

Simulink is a model based design environment that allows you to model a system, simulate its behaviors and refine your design before implementation. With simulink simulations, you can ensure that the system performs to your specifications, explore design tradeoffs and tune parameters to optimize performance. In this section the fig (4) shows the desensitized half band filter realized using the basic filter building blocks along with results. This is implemented from equation (5) and we use these results to compare with Xilinx simulation results. Here filter's tap coefficient values $a_0, a_1, a_2,\ a_3$ are calculated from equation (3) with $h_0 = 8192,\ h_1 = 4964,\ h_3 = -1102,\ h_5 = 273,\ h_7 = -39$. In fig.4 the input to the filter are discrete signals which are generated by using the used defined functional block in simulink and the inputs are displayed in display block and outputs are displayed in the display1 block. Later these results are compared with Xilinx simulation results.

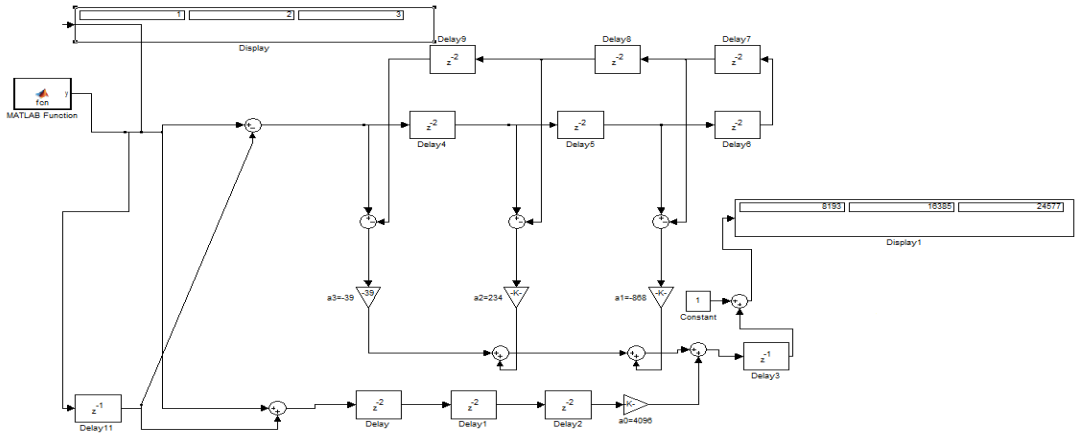

Figure 4:Implementation of 15-tap desensitized half band filter in simulink

IV. FPGA IMPLEMENTATION

Very high speed hardware description language (VHDL) has strong abstract description ability to support hardware design, verification, synthesis and testing. VHDL can describe the same logic function in multiple levels, such as it can describe the structure of the circuit composition in the register level and describe the function and performance of the circuit in the behavior level. VHDL has been used to enter hardware description of low pass FIR half band filter. The implementation has been done on a FPGA platform. The filter design has been prototyped on an xc6vcx240t-1ff1156 FPGA device in vertex 6 Platform using ISE 14.2.

SIMULATION RESULTS

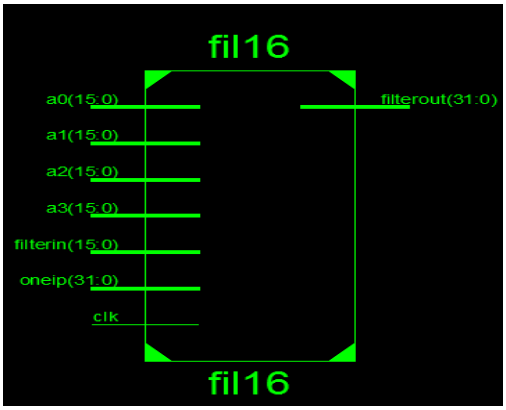

Figure 5:Top level block of 15-tap desensitized half band filter on Xilinx ISE 14.2

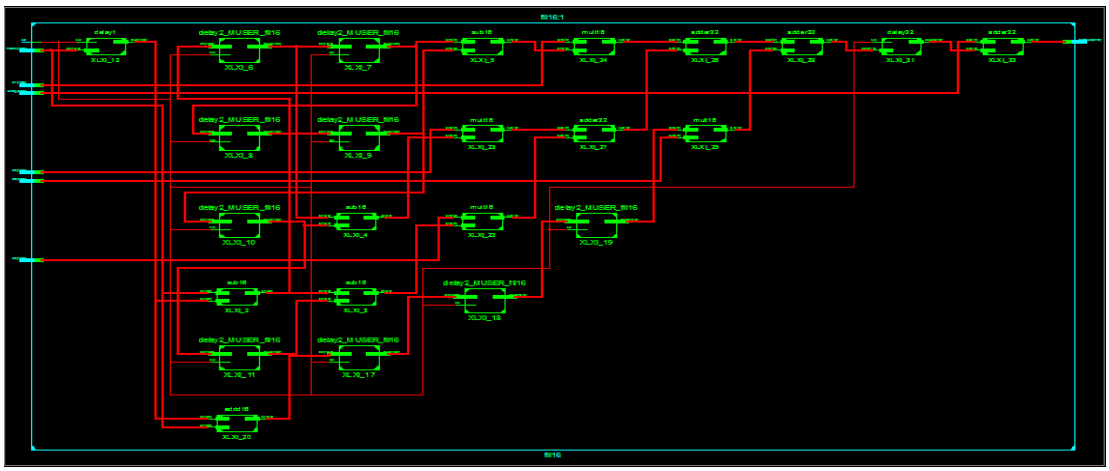

Figure 6: rtl schematic of 15-tap desensitized half band filter on Xilinx ISE 14.2

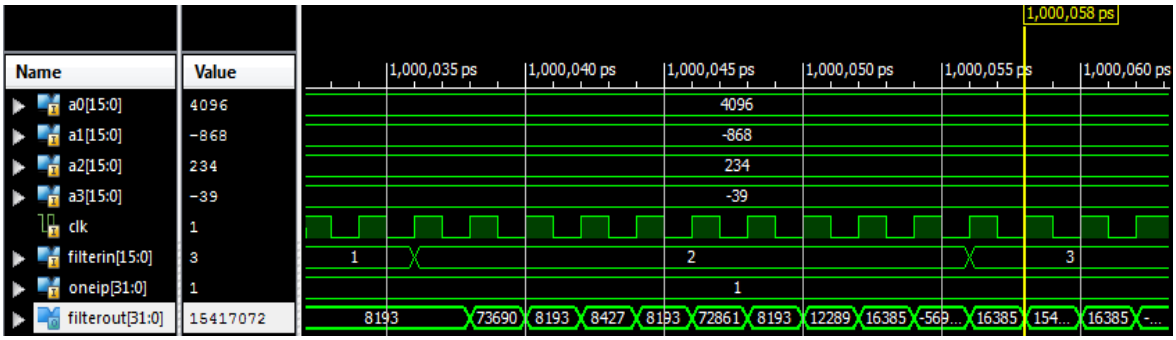

Figure 7: simulation results of 15-tap desensitized half band filter on Xilinx ISE 14.2

Table 1: Resource utilization of 15-tap desensitized half band filter on Xilinx ISE 14.2

Logic Utilization	Used	Available	Utilization
Number of Slice Registers	41	301440	0%
Number of Slice LUTs	56	150720	0%
Number of fully used LUT-FF pairs	22	75	29%
Number of bonded IOBs	37	600	6%
Number of BUFG/BUFGCTRLs	1	32	3%
Number of DSP48E1s	4	768	0%

V. CONCLUSION

This paper mainly describes the design and implementation of lowpass FIR half band filter which is based on FPGA, Xilinx tools, matlab and simulink. The results obtained from simulink and FPGA implementation are similar. These half band filters can be used in digital down converter in SDR. Adders used are ripple carry adders, further optimization can be achieved by using other adders with less design time.

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BIOGRAPHIES

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